REMARKS

Claims 1-3 are all the claims pending in the application. By this Amendment, Applicant amends claim 1 to further clarify the invention.

Preliminary Matters

As a preliminary matter, the Examiner did not acknowledge the claim to foreign priority and the receipt of a certified copy of the priority document. Therefore, the Examiner's acknowledgement of the claim to foreign priority and confirmation that the certified copy of the priority document was received is respectfully requested.

Moreover, the Examiner objected to the Drawings for failing to label Figures 3, 4A, and 4B --prior art--. Applicant labels Figures, 3, 4A, and 4B --prior art--. Replacement Drawings are accompanying this response. As a result, the Examiner is respectfully requested to acknowledge receipt and indicate approval of the drawing corrections in the next Patent Office paper.

Finally, the Examiner failed to consider the Information Disclosure Statement filed on November 6, 2000. In fact, the Examiner has crossed out the reference listed on the Form PTO-1449 submitted with the Information Disclosure Statement filed on November 6, 2000. In accordance with MPEP § 609, however, the catalogue has been adequately identified by providing the title, the publisher and the date of publication. Moreover, a translation of the catalogue has also been provided. Therefore, it is appropriate and necessary for the Examiner to consider the catalogue and to initial this reference as listed on the Form PTO-1449. For Examiner's convenience, Applicant encloses a copy of the Form PTO-1449.

Summary of the Office Action

The Examiner withdrew the previous rejections. The Examiner, however, found new grounds for rejecting claims 1-3. In particular, the Examiner now rejected claims 1 and 2 under 35 U.S.C. § 102(b) in view of a newly found reference and claim 3 under 35 U.S.C. § 103(a).

AMENDMENTS TO THE DRAWINGS

The attached two (2) sheets of Drawings include the following changes:

In Figures 3, 4A and 4B are labeled "Prior Art".

Attachment: Replacement Sheets (2)

Rejections under 35 U.S.C. § 102

Claims 1 and 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,555,225 to Hayashi (hereinafter "Hayashi"). The Examiner's careful reconsideration is submitted to be appropriate in view of the following comments traversing the rejection.

To be an "anticipation" rejection under 35 U.S.C. § 102, the reference must teach ***every element and recitation of the Applicant's claims***. Rejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. Thus, the reference must clearly and unequivocally disclose every element and recitation of the claimed invention.

Of the rejected claims, only claim 1 is independent. Independent claim 1, among a number of unique features, recites: "a pulse dividing section for dividing the pulse string output from said pulse generating section at a predetermined dividing ratio and for outputting an interruption request signal having a cycle which is n times as great as the cycle of the pulse string...wherein the pulse dividing section determines the interruption request signal based on the dividing of the pulse string output." The Examiner alleges that Hayashi's frequency divider 4 and memory 3 combined are equivalent to the pulse dividing section as set forth in claim 1 (page 3 of the Office Action).

Hayashi teaches a microcomputer 1 with a clock generating circuit 5a outputting a pulse and a frequency divider 4 which divides the frequency of an oscillating voltage outputted through the clock output terminal Xout of the clock generating circuit 5a and inputs the divided frequency into the CPU 2 (col. 4, lines 1 to 9; col. 4, lines 47 to 54). In particular, the frequency from the clock generating circuit 5a is divided by the frequency divider 4 down to a clock frequency inherent in the microcomputer 1 (col. 5, lines 15 to 21). Hayashi further teaches that the CPU 2 exchanges data with memory 3 in accordance with the clock frequency and arithmetically processes the data (col. 5, lines 24 to 30).

In particular, Hayashi addresses the problem of malfunctions occurring in the CPU which result in stopping the clock generator and thus discontinuing the operation of the microcomputer. In Hayashi, however, microcomputer 1 continues to operate even when the CPU malfunctions

(col. 2, lines 15 to 30 and lines 55 to 60). In particular, this is accomplished by having a clock generator with a first memory for storing a first signal outputted by the CPU and a first matched signal generating circuit for outputting a second signal permitting the suspension of clock oscillation when the content of the memory stored in the first memory is found in accord with the memory stored therein.

Moreover, in Hayashi, the signal generating circuit has a second memory for storing a third signal from the CPU and a second matched signal generating circuit for providing a fourth signal suspending the clock oscillation to the clock oscillator when the content of the memory stored in the second memory is found in accord with the memory stored therein. Also, the signal generating circuit has a gate circuit for permitting the second memory to store the third signal in response to the second signal outputted by the first matched signal generating circuit. When the first signal stored in the first memory is in accord with a predetermined signal, and the third signal stored in the second memory is in accord with a predetermined signal, the second matched signal generating circuit outputs the fourth signal, the clock oscillation is suspended (col. 2, line 61 to col. 3, line 30).

In Hayashi, however, in order to execute a stop request, the divider 4 outputs divided frequency ***to the CPU***, which processes this divided frequency by exchanging data with the memory 3. In other words, in Hayashi, the divided frequency is first output to the CPU and then ***the CPU decides whether to request a stop order from the memory 3***. In other words, the clock divider outputs the divided frequency to the CPU and then the CPU processes the frequency to determine whether to request a stop order from the memory 3. Hayashi fails to teach or suggest having the pulse dividing section determine the interruption request based on the dividing of the pulse string output. In Hayashi, it is ***the CPU that receives the dividing frequency and determines whether to request a stop order*** from memory 3.

In short, even if Hayashi's memory and frequency divider is somehow compared to the pulse dividing section as set forth in claim 1, Hayashi still fails to teach or suggest a pulse dividing section configured to determine the interruption request signal based on the dividing of

the pulse string output. In Hayashi, the divided frequency is inputted into the CPU and the CPU determines whether to request a stop order.

Moreover, claim 1 recites: "a central processing unit for executing an interruption processing in response to the interruption request signal output from said pulse dividing section so as to directly control the output of said pulse generating section." The Examiner alleges that Hayashi's CPU directly controls the clock generating circuit 5a (see pages 3-4 of the Office Action).

In Hayashi, however, the purpose of the invention is to prevent direct control by the CPU of the clock generating section. In other words, Hayashi addresses the problem of malfunctioning CPU stopping the clock generating section 5a. To prevent this from happening, a special check is executed in the clock generating circuit 5a. In particular, only when the first signal stored in the first memory is in accord with a predetermined signal, and the third signal stored in the second memory is in accord with a predetermined signal, the second matched signal generating circuit outputs the fourth signal whereby the clock oscillation is suspended (col. 2, line 61 to col. 3, line 30). In other words, in Hayashi, the clock generating circuit 5a ***is not directly controlled by the CPU since the clock generating circuit 5a checks the output of the CPU*** to verify that the suspension of operation is in fact desired and is not a result of a runaway (malfunctioning) CPU.

Therefore, "a pulse dividing section for dividing the pulse string output from said pulse generating section at a predetermined dividing ratio and for outputting an interruption request signal having a cycle which is n times as great as the cycle of the pulse string...wherein the pulse dividing section determines the interruption request signal based on the dividing of the pulse string output" and "a CPU for executing an interruption processing in response to the interruption request signal output from said pulse dividing section so as to directly control the output of said pulse generating section," as set forth in claim 1 is not disclosed by Hayashi, which lacks having a pulse dividing section outputting an interruption request determined by the pulse dividing section based on the dividing of the pulse string, and Hayashi lacks the CPU which directly controls the clock circuit generator. In Hayashi, the generator checks the signals

output by the CPU for accuracy and only if the CPU's signal is verified, then the generator output results in accordance with the CPU request.

For at least these exemplary reasons, claim 1 is patentably distinguishable from Hayashi. Therefore, it is appropriate and necessary for the Examiner to withdraw this rejection of independent claim 1. Claim 3 is patentable at least by virtue of its dependency on claim 1.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected Claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Hayashi in view of Gupta. This rejection is respectfully traversed with respect to the claim 2 which depends on claim 1. It was already demonstrated that Hayashi does not meet all the requirements of independent claim 1. Gupta is relied upon only for its teaching of the CPU controlling the number of pulses output from said pulse generating section and for setting the dividing ratio.

In general, Gupta teaches a microprocessor having software controllable power consumption which adjusts the rate of execution of a functional init by removing power to the functional unit so that the power consumption is reduced. In particular, in Gupta, the global power control register field adjusts the rate of execution of all the functional units by controlling the clock frequency supplied to all the functional units. In addition, Gupta teaches a clock divider that divides down the master clock signal response to the value stored in the power control register field.

Gupta clearly fails to cure the deficient teachings of Hayashi. Gupta fails to teach or suggest having a pulse dividing section output an interruption request signal to the CPU. Moreover, Gupta fails to teach or suggest having the pulse dividing section determine the interruption request signal based on the dividing of the pulse string. Moreover, Gupta fails to directly control the clock generation section in response to the interrupt request from the dividing circuit.

In short, the combined teachings of Hayashi and Gupta, taken together for what they would have meant to the artisan of ordinary skill, thus fail to meet the requirements of claim 1.

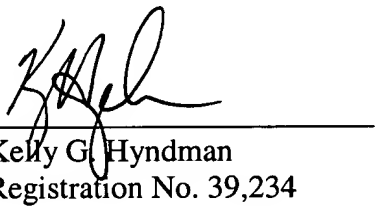
Therefore, it is respectfully submitted that claim 2 is patentable at least by virtue of its dependency on claim 1.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: October 27, 2004

47

FILING RECEIPT
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In re application of

YOKOKAWA, SHINSUKE

Appln. No. 09/635,561 Group Art Unit: 2786

Filed: August 10, 2000 Examiner: *not yet assigned*

For: PROGRAMMABLE CONTROLLER

PAPER(S) FILED ENTITLED:

1. Information Disclosure Statement (with reference and PTO Form 1449)

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ATTORNEY/SEC: RCT:te

Date Filed: November 6, 2000

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

YOKOKAWA, SHINSUKE

Appln. No. 09/635,561 Group Art Unit: 2786

Filed: August 10, 2000 Examiner: *Not yet assigned*

For: PROGRAMMABLE CONTROLLER

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached Form PTO-1449 and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

A copy of the listed document is submitted herewith.

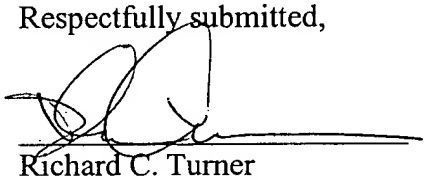
The present Information Disclosure Statement is being filed (1) no later than three months from the application's filing date or (2) before the mailing date of the first Office Action on the merits and therefore no Statement under 37 C.F.R. § 1.97(e) or fee under 37 C.F.R. § 1.17(p) is required.

INFORMATION DISCLOSURE STATEMENT
U.S. Appln. No. 09/635,561

In compliance with the concise explanation requirement under 37 C.F.R. § 1.98(a)(3) for foreign language documents Applicant submits the attached translation. A copy of the original catalogue sheets is attached for the Examiner's convenience.

The submission of the listed document is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

Respectfully submitted,



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Form PTO-1449 (Rev. 2-32) U.S. Department of Commerce Patent & Trademark Office	Atty. Docket No. Q60393	Serial No. 09/635,561
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant: YOKOKAWA, SHINSUKE	
	Filing Date: August 10, 2000	Group: 2786

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub-Class	Filing Date (if appropriate)

FOREIGN PATENT DOCUMENTS

		Document	Date	Country	Class	Sub-class	Translation Yes/No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		"Mitsubishi Sequencer Catalogue, Mitsubishi Denki K.K., October, 1999

EXAMINER: DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication.